How to make a Quick Turn PCB that modern RF parts will actually fit on!

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I like to use those low cost, no frills or "Bare Bones" [1] type of PCB for prototyping as they are fast and easy to design and get made. I can design a board in a few hours with nearly any CAD package (even the free ones) and have a PCB on my desk in 2 days for very little money. This is just a superb way to test out circuit ideas in real hardware for very little investment in time and money.

The problem is with RF circuits. To prototype RF circuits the traces must usually be made 50 ohms for proper operation of the circuit. Every year our parts get smaller but the laws of Physics don't change. This means that a Microstrip trace on a 0.062 inch thick standard prototype board that was calculated to be 0.110 inches wide thirty years ago is still 0.110 inches wide today. But many SMT parts aren't this big any more, much less their lead spacing, so it would seem that the low cost 2 layer prototype boards for RF prototyping are not suitable for today's small SMT parts, or are they?

There are other structures for building 50 ohm RF traces on PCB's than simply resorting to Microstrip lines. One such method originally popularized by the IC Guru's is a Coplanar Waveguide or what we will be using here, specifically a Coplanar Waveguide over Ground (or CPWG). A CPWG structure has the attributes of narrowing the required trace width compared to a regular Microstrip structure (keeping all the other dimensions the same).

Think about it this way, if a grounded copper plane on the topside of the board is brought closer to a Microstrip trace then we have added capacitance to the Microstrip structure. To compensate for this added capacitance and to keep the entire structure 50 ohms we need to make the center trace more inductive – specifically by making it narrower. We can keep doing this: Making the ground plane closer and narrowing the line width until we reach the limits of our fabrication technology or some other convenient number of trace width and topside ground plane gap.

The trick is: "How do we go about designing the CPWG structure for our low cost and fast PCB process?". You can find many CPWG calculators out there on the web, but to my knowledge they all fail when the ground plane gap gets less than about 30 to 50% of the trace width. Why? Because the height of the copper traces on the board begins to be a significant factor and adds much more capacitance than the calculators assume. Hence the lines that they design are more and more capacitive and end up being much, much less than 50 Ohms. Remember I said the IC Gurus first started using the CPW and CPWG structures? Well the equations date back to them and let's face it, a layer of

Aluminum on a GaAs substrate is pretty thin compared to the 0.002 inch or more thick 2 ounce copper on our finished prototype PCB's. So these “Popular Equations” work for IC's and their physical structures, but fall apart because our PCB's are much different physically.

The only way to my knowledge to actually properly design a CPWG on a PCB with very narrow gap to center trace ratios is to use a full 3D Electromagnetic simulator.

Those are expensive tools, but not to worry. The purpose of this design note is to let you know what the values are for a few common types of structures.

In keeping with the minimum trace to trace spacing of 6 mils a CPWG structure was simulated, built and tested. For a common 0.062 inch thick FR-4 PCB material – A trace width of 0.032 inch with a gap of 0.006 inch is as close to 50 Ohms as you can get (better than 40 dB return loss on the trace at 6 GHz and that's really good) (See Figure 1).

This is much more usable than the 0.110 inch trace width and is actually compatible with SMT sized parts. A 0603 sized SMT part fits this line perfectly and a common SMA Edge Launch connector [2] also fits the line perfectly.

Figure 2 shows a picture of several common RF type parts in comparison to the fabricated PCB.

If you have a part with larger pad dimensions than the 0.032 inch trace width just increase the spacing to the top ground plane to compensate. For instance: On a 0805 SMT pad increase the spacing to the top plane to about 0.008 to 0.012 inch, and for a 1206 SMT component pad increase the top plane spacing to 0.012 to 0.016 inch to keep the pad from being too capacitive. The Exact value depends on how big the Pad really is, these values are for the IPC Least pad size. I always use IPC Least pad dimensions for RF work.

The PCB's that I tested had the copper planes pulled back 0.010 inch from the routed board edge (A common design rule). This coupled with the Edge Launch connector adds some slight inductance to the transition. Not to worry, that big center pin of the Edge Launch Connector on top of the trace adds extra capacitance, so you have a built in capacitive compensation. I have found that if you cut the pin to about one third it's original length you will get about equal capacitance to balance the transition inductance.

The CPWG structure needs solid ground plane under the trace and the top ground plane needs to be “Stitched” to the bottom ground plane with Vias. There must not be any cutouts in the bottom ground plane under the topside trace or you will add a large amount of inductance to the structure and the high frequency performance will suffer. The stitching Vias must be placed less than 1/8th of a wavelength of the highest frequency that you will be working at. I usually use 0.100 inch spacing and this will work

well out to past 10 GHz.

Spacing of the stitching Vias to the center trace follows the same spacing rules. Don't stress out too much about this, it is easy to get enough Vias in and around the trace to make this work out well.

If you don't have enough Vias you will see slight, but rapid 0.5 to 1 dB drop in the S21 transmission characteristics instead of a nice linear loss slope with frequency. The effect is instantly noticeable on a Vector Network Analyzer S21 measurement (See figure 3).

I have measured the test board and it has about 0.25 dB of loss per inch at 3 GHz and 1 dB of loss per inch at 10 GHz, including two Edge Launch connectors, pretty respectable for a low cost prototype PCB.

If you need to interface to a SMT part or IC that has narrower pads than 0.032 inch, just neck down the center conductor as close to the part as possible. Remember the effect of these impedance discontinues increases as their size increases and with increasing frequency. So if your discontinuity is small in physical size it will have little effect until very high frequencies.

Appendix A – Quick turn 0.020 inch thick Rogers RO4350B

At least one supplier [3] is now making to layer quick turn prototypes using the very nice and very high performance Rogers RO4350B material in 0.020 inch thickness. In line with the above discussion I have designed and tested a suitable CPWG structure using this material. To make a 50 Ohm line using this material I found that pretty much optimum is to use a 0.032 inch line width with a 10 mil gap on each side. This gives a very nice 50 ohm line with low loss. A higher performance edge launch connector can be used to get higher frequency performance that this material affords [4].

Appendix B - A 0.050 Inch trace width on 0.062” thick FR-4

Some RF Modules have very big landing pads, sized to mate with 0.050 inch wide lines. A CPWG over ground design for these instances is to increase the Gap to 12 Mils. This gives a very nice 50 Ohm Line.

[1] See www.barebonespcb.com for one such supplier.
[2] Johnson Edge Launch P/N: 142-0711-821
[3] See www.sunstone.com for one such supplier
[4] Johnson Edge Launch P/N: 142-0761-861

Note: A shortened version of this article was first published in EDN, December 15, 2010

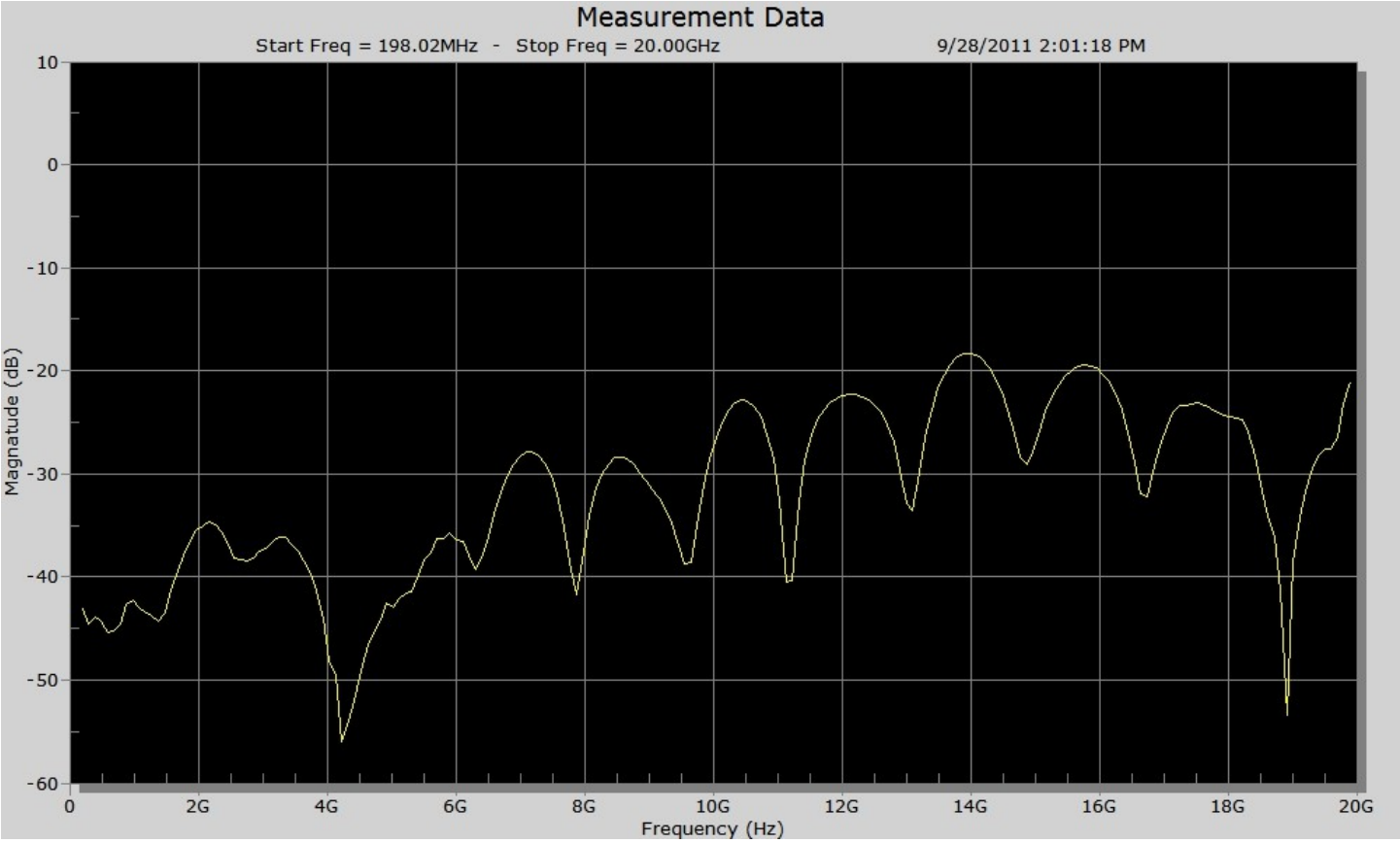

Figure 1 – Here is a S11 measurement of a 2 inch long, FR-4 test board. The S11 measurement also included the mismatch of the two SMA connectors [4]. If the connectors are "Gated Out" of the measurement the S11 of the trace alone is better than -40 dB up to 8 GHz.

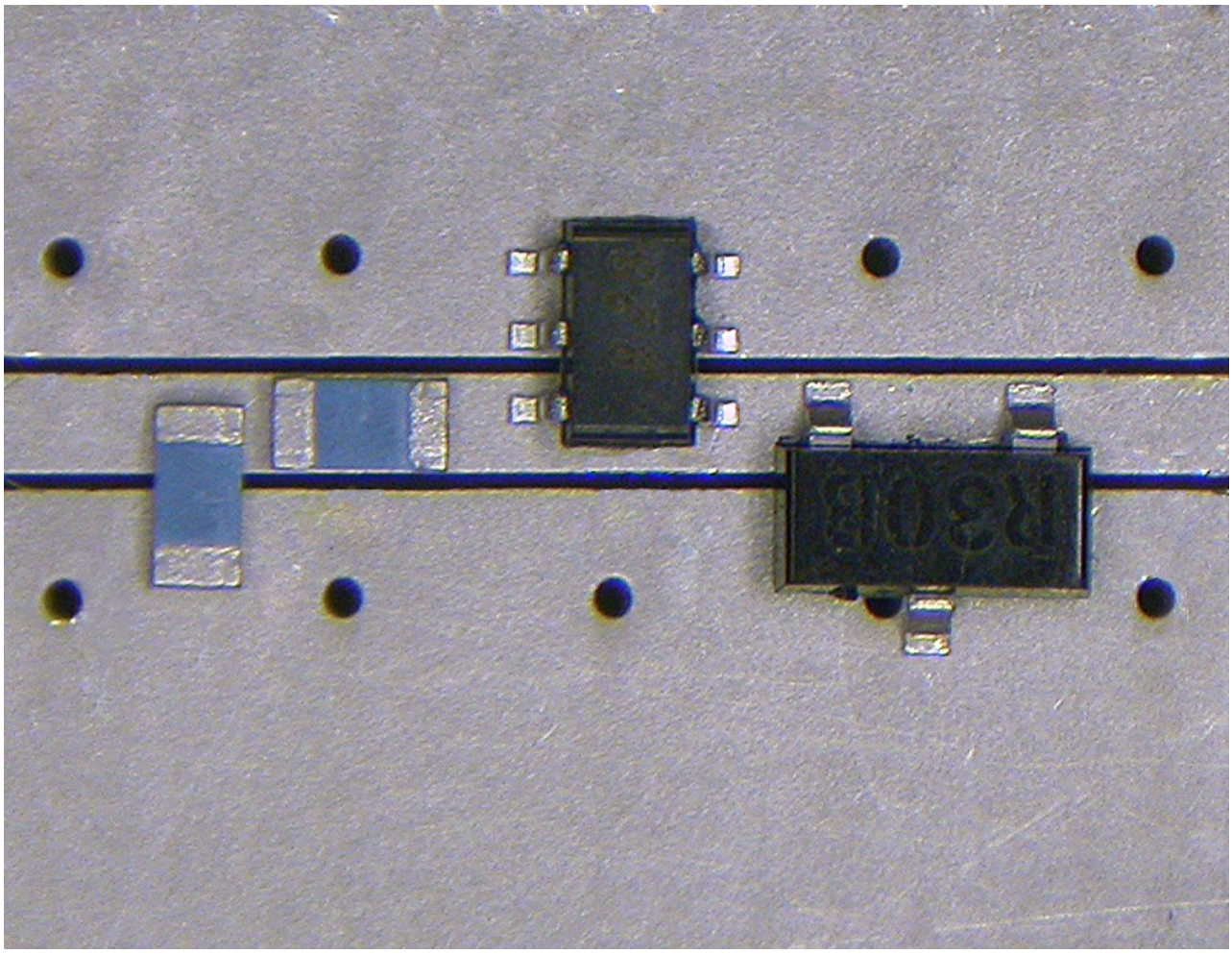

Figure 2 – A sampling of nominally small SMT parts showing how well they fit on the small 0.032 inch wide CPWG 50 Ohm line structure. 0603 resistors and capacitors fit perfectly, a small GaAs FET Amplifier IC (SC-70) fits fine on this sized line and also shown for comparison is a standard SOT-23 package (in which a lot of PIN and switching diodes are packaged). The stitching Vias at 0.100 inch spacing can also be seen.

Please note: The top Ground plane really doesn't have to extend past the row of Vias as all the significant RF current flows to the Vias and not beyond. Sometimes in very tight circuit situations the stitching Vias may have to be put in at odd intervals – don't worry too much about this for normal designs – you circuit will still (in all likelihood) function well.

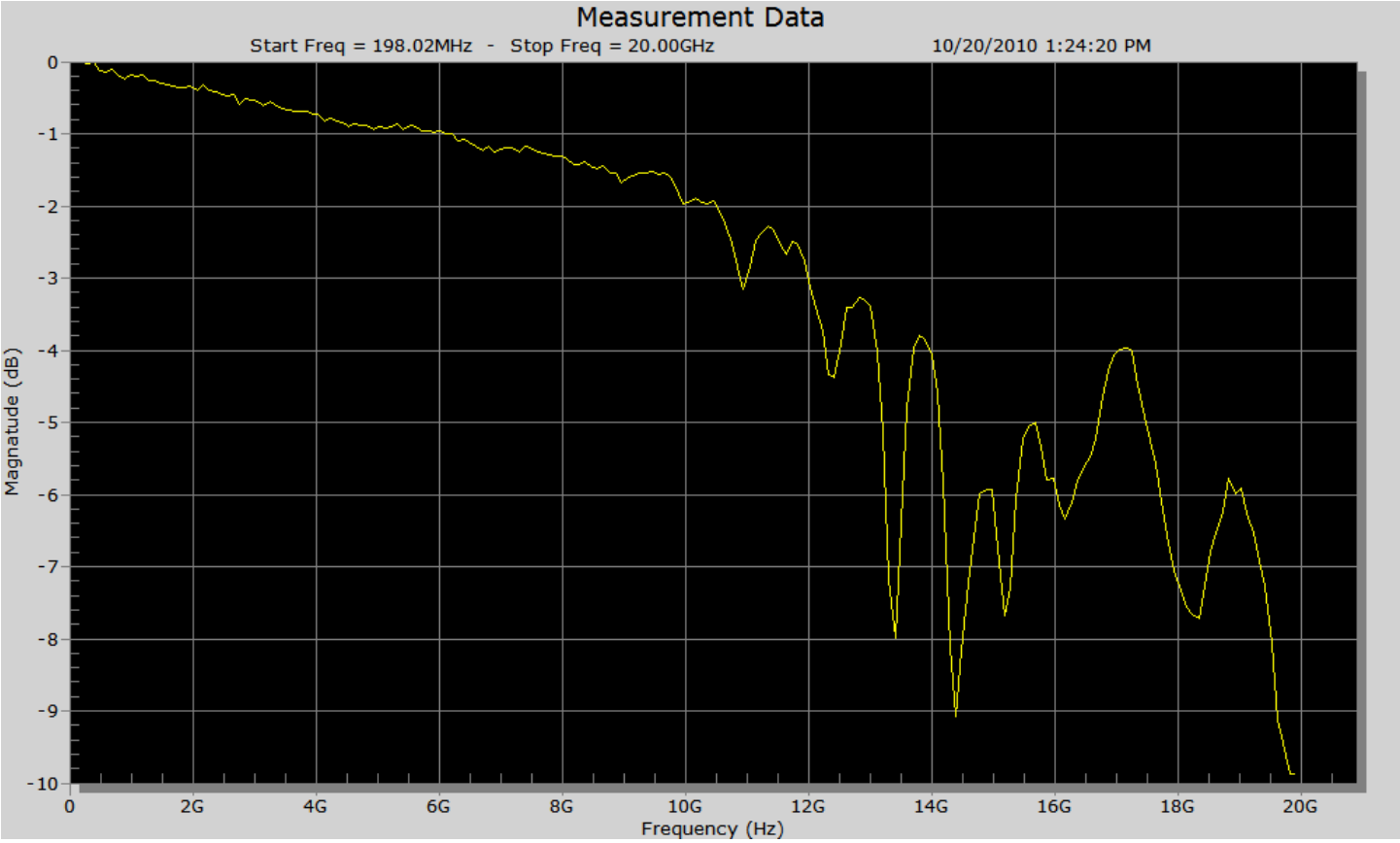

Figure 3 – Can you spot the trouble here? In this S21 (Through) measurement the Vias are spaced at 0.2” along the line – this spacing works fine up to about 9 GHz then the resonances caused by the large gap between the stitching Vias start to show up. Instead of following the nice smooth linear loss versus frequency this test circuit shows increasing deviations and pretty substantial suck-outs as the frequency increases.

If in doubt as to if you got the via spacing right on a CPWG structure, just do a S21 measurement to find out for sure. This problem isn't shy and will show right up!

Note: This test was the entire 2 inch of the test line with 0.2 inch Via spacing. If the spacing had been 0.1 inches or smaller then the trouble would have started even farther out in frequency. Likewise if only one Via was missing in a closely packed set – you would have to look very hard indeed to spot any trouble.

So as I said: Don't stress out too much as to perfect via spacing – it really is pretty easy to get enough stitching Vias for our typical 6 GHz and under wireless circuits so that everything works out just fine.

As the song says: “Don't worry – be happy” (And don't stress over exact Via spacing).

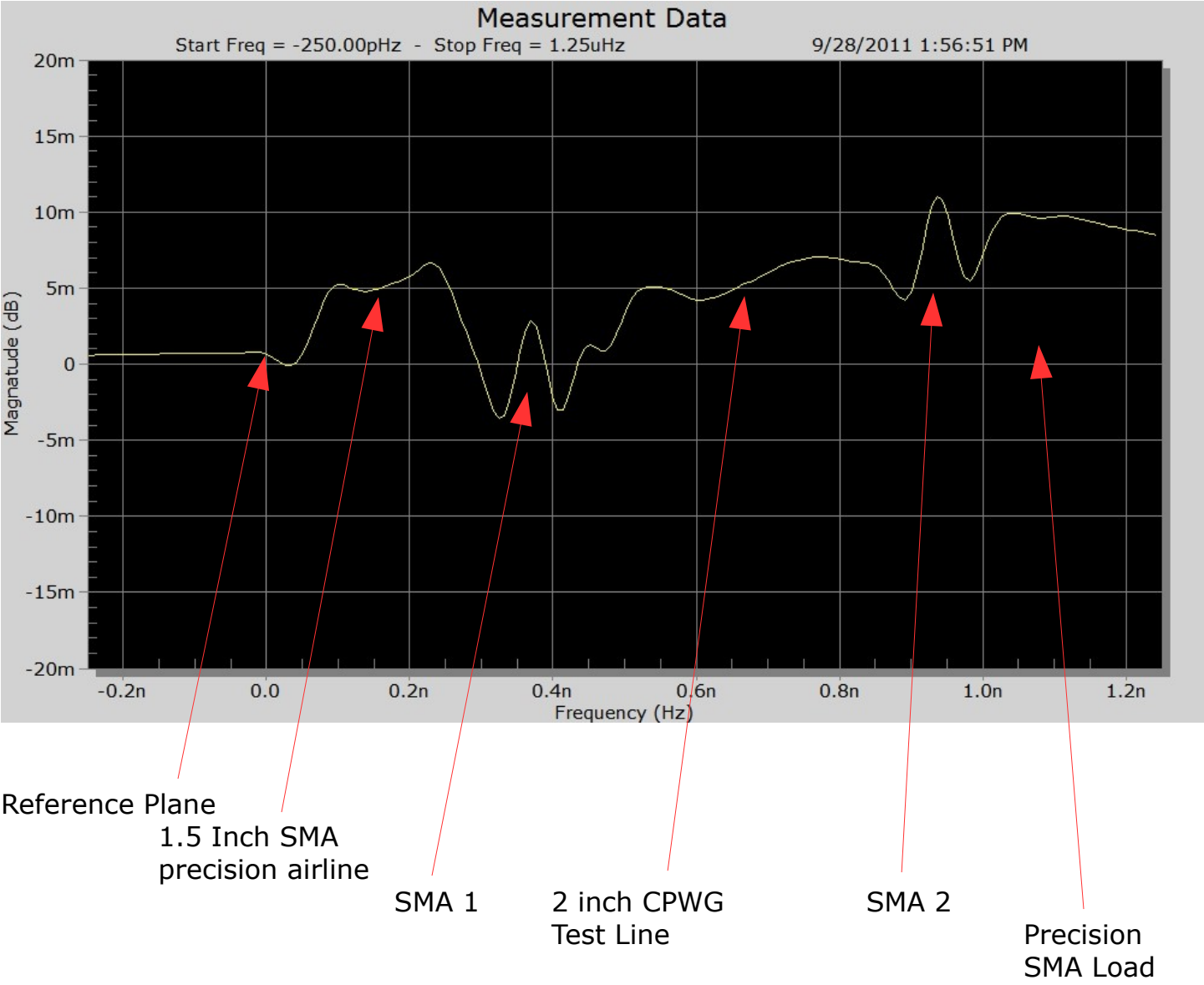

Figure 4 – This shows the TDR plot of the response of the board used for figure 1. Features are called out as shown. As can be seen the CPWG test line has about the same amplitude as the precision airline, indicating that the test line impedance is very close to 50 ohms (the impedance of the airline). Note: The horizontal, X Axis is really in Nanoseconds, not Hz as shown on the plot.